Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-47 (Cancelled)

48. (New): A universal interface module, comprising:

transmit control logic, the transmit control logic is configured to receive a signal indicative of the type of transceiver coupled to the module;

an output interface, the output interface comprising a control input, a data input, a control output and a data output; and

an output register coupled between the transmit control logic and the control input of the output interface;

wherein the data input of the output interface is coupled to a data stream to be output by the output module, the control output and data output are coupled to the transceiver; and

wherein the transmit control logic is responsive to the signal indicative of type of transceiver is coupled to the module to issue control codes to the output register, the output register responsive to the control codes to send control codes to the output register based on the control codes received from the transmit control logic; and

wherein the output interface is responsive to a signal indicative of the type of transceiver coupled to the module to format signals from at least one of the control output and the data output accordingly.

49. (New): A universal interface module according to claim 48, further comprising a function mapping register coupled between the control logic and the control input of the output register.

50. (New): A universal interface module according to claim 48, the output interface further comprising a data formatter that receives the data stream from the data input, and inserts idle message precursor information and normal message precursor information into the data stream.

51. (New): A universal interface module according to claim 50, further comprising:

the data formatter further configured to receive delimiter signals from the transmit control logic; and

wherein the data formatter is configured to be responsive to receipt of the delimiter signals to insert the delimiter signals into the data stream.

52. (New): A universal interface module according to claim 48, further comprising:

the transmit control logic is operable to send a two bit control word to the output register, the two bit control word indicative of which of a group consisting of four, three bit control words, are to be output from the output register to the output interface.

53. (New): A universal interface module according to claim 48, wherein when the data stream is a low voltage differential signal, the output interface receives parity and control bit information that is transmitted in parallel with the data stream to the transceiver.

54. (New): A universal interface module according to claim 48, further comprising:

the transmit control logic adapted to receive a delimitation control signal, an initialize word sync event signal and an idle character insertion signal;

wherein the transmit control logic is responsive to the delimitation control signal, initialize word event signal and idle character insert signal to instruct the output register to provide the proper signals to the control input of the output interface to format the control output of the output interface.

55. (New) A universal interface module, comprising:

an input register adapted for receiving a control data stream from a transceiver;

receive control logic coupled to the input register; and

an input module interface module adapted to receive control data from the receive control logic and a data stream from the transceiver, and a signal from the transceiver indicative of the type of transceiver that is coupled to the module, the input module interface having a control and parity output and a data output;

wherein the input module interface module is responsive to the signal from the transceiver to convert at least one of the data stream and the control data accordingly.

56. (New): A universal interface module according to claim 55, further comprising delay logic adapted for synchronizing the control stream with the data stream.

57. (New): A universal interface module according to claim 55, further comprising:

the input module interface logic comprises a control signal deformatter for converting the control stream for downstream use.

58. (New): A universal interface module according to claim 57, further comprising:

the input module interface logic comprises a data deformatter for converting the data stream for downstream use.

59. (New): A universal interface module according to claim 58, further comprising:

the input module interface logic further comprises

a first input having associated delay logic

a second input for bypassing the associated delay logic;

wherein the input module interface logic is responsive to the signal from the transceiver indicative of the type of transceiver that is coupled to the module to select one of the first input and the second input to forward to the data deformatter.

60. (New): A universal interface module according to claim 59, further comprising:

a comparator coupled to the delay logic of the first input adapted for detecting at least one of idle message precursor and normal message precursor codes that forwards the at least one of idle message precursor and normal message precursor codes to the receive control logic.